

REMARKS

The Office Action dated December 12, 2006, has been received and carefully noted. The above amendments and the following remarks are being submitted as a full and complete response thereto. Claims 1-8, 12-20, and 23 are pending in this application. By this amendment, claims 1, 6, 12, 17, 19, and 20 are amended. The claim amendments are fully supported in the specification as originally filed, for example, at page 15, paragraph [0080]. No new matter has been added. Reconsideration of the application is respectfully requested.

The Office Action rejects claims 1, 4-6, 8, 12, 14-17, 19, and 20 under 35 U.S.C. § 102(b) as being anticipated by Sha et al. (U.S. Patent No. 6,404,294); and claims 2, 3, 7, 13, 18, and 23 under 35 U.S.C. § 103(a) as being obvious over Sha in view of Fig. 1 of Applicant's Admitted Prior Art ("AAPA"). The rejections are respectfully traversed.

The above-identified application claims a clock generator circuit comprising a phase comparator receiving a standard clock signal and an operating clock signal and generating an output signal, and a voltage controlled oscillator generating the operating clock signal based on the output signal of the phase comparator, wherein the voltage controlled oscillator comprises a voltage current converter converting a voltage signal into a current signal, a current D/A converter fluctuating the current signal based on a digital signal, and a current controlled oscillator oscillating the operating clock signal of which frequency corresponds to each of the variable current signals, wherein the current D/A converter has a plurality of current sources including current mirror circuits, as recited in independent claim 1 and similarly recited in independent claims 6, 12, 17, 19 and 20.

Sha teaches an apparatus comprising a first circuit configured to generate an output signal having a frequency that varies in response to a voltage signal and a load, and a second circuit configured to generate the load by coupling one or more resistive devices to a reference node in response to a control signal (Abstract). However, nowhere in Sha is there a teaching of a current D/A converter having a plurality of current sources including current mirror circuits, as recited in the independent claims. Thus, Sha fails to disclose or suggest each and every feature of independent claims 1, 6, 12, 17, 19 and 20. To qualify as prior art under 35 U.S.C. § 102, a single reference must teach, i.e., identically describe, each feature of a rejected claim. For at least the reasons provided above, Sha does not teach or suggest each and every feature recited by claims 1, 6, 12, 17, 19, and 20. Accordingly, claims 1, 6, 12, 17, 19, and 20, and their dependent claims, are patentable over Sha.

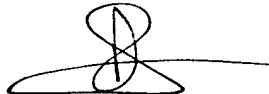
AAPA is a diagram of a conventional PLL clock generation circuit that oscillates by generating a semiconductor operating clock (paragraph [0003]). However, AAPA fails to cure deficiencies in Sha in disclosing or rendering obvious the features of independent claims 1, 6, 12, 17, 19 and 20. Thus, claims 1, 6, 12, 17, 19 and 20, and their dependent claims, are patentable over a combination of Sha and AAPA.

For at least the reasons discussed above, claims 1, 6, 12, 17, 19, and 20, and their dependent claims, are allowable over all the applied references. Thus, withdrawal of the rejections of the claims under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) is respectfully requested.

The Applicant respectfully submits that this application is in condition for allowance and such action is earnestly solicited. If the Examiner believes that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below to schedule a personal or telephone interview to discuss any remaining issues.

In the event that this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to Counsel's Deposit Account Number 01-2300, referencing Docket Number 100698-00014.

Respectfully submitted,



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